

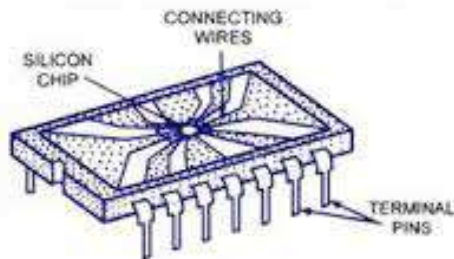
MONOLITHIC INTEGRATED CIRCUITS AND ITS APPLICATION



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MONOLITHIC IC'S



Monolithic IC in Plastic Package

Monolithic circuit is built into a single stone or single crystal i.e. in monolithic ICs, all circuit components, and their interconnections are formed into or on the top of a single chip of silicon. Monolithic ICs are by far the most common type of ICs used in practice, because of **mass production** , **lower cost** and **higher reliability**.

INTEGRATED CIRCUITS

- An integrated circuit (IC) is a miniature ,low cost electronic circuit consisting of active and passive components fabricated together on a single crystal of silicon.
- The active components are transistors and diodes and passive components are resistors and capacitors.

Advantages of integrated circuits

1. Miniaturization and hence increased equipment density.
2. Cost reduction due to batch processing.
3. Increased system reliability due to the elimination of soldered joints.
4. Improved functional performance.
5. Matched devices.
6. Increased operating speeds.
7. Reduction in power consumption

CLASSIFICATION OF ICs

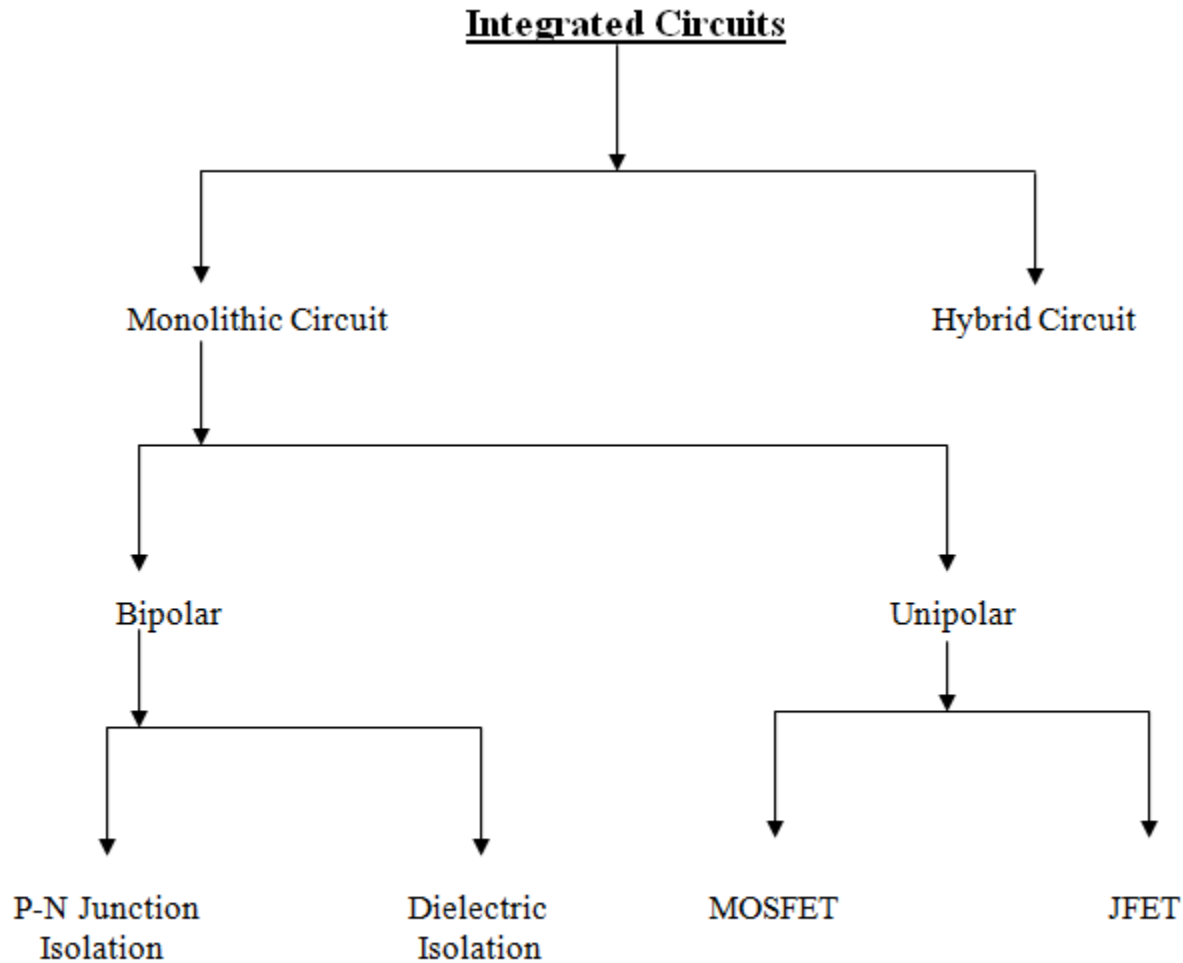
Integrated circuits offer a wide range of applications and could be broadly classified as:

- 1. Digital ICs**
- 2. Linear ICs**

Based on these two requirements. Two distinctly different IC Technology namely

- 1. Monolithic Technology and**
- 2. Hybrid Technology**

CLASSIFICATION OF ICs



Classification of ICs

Monolithic IC

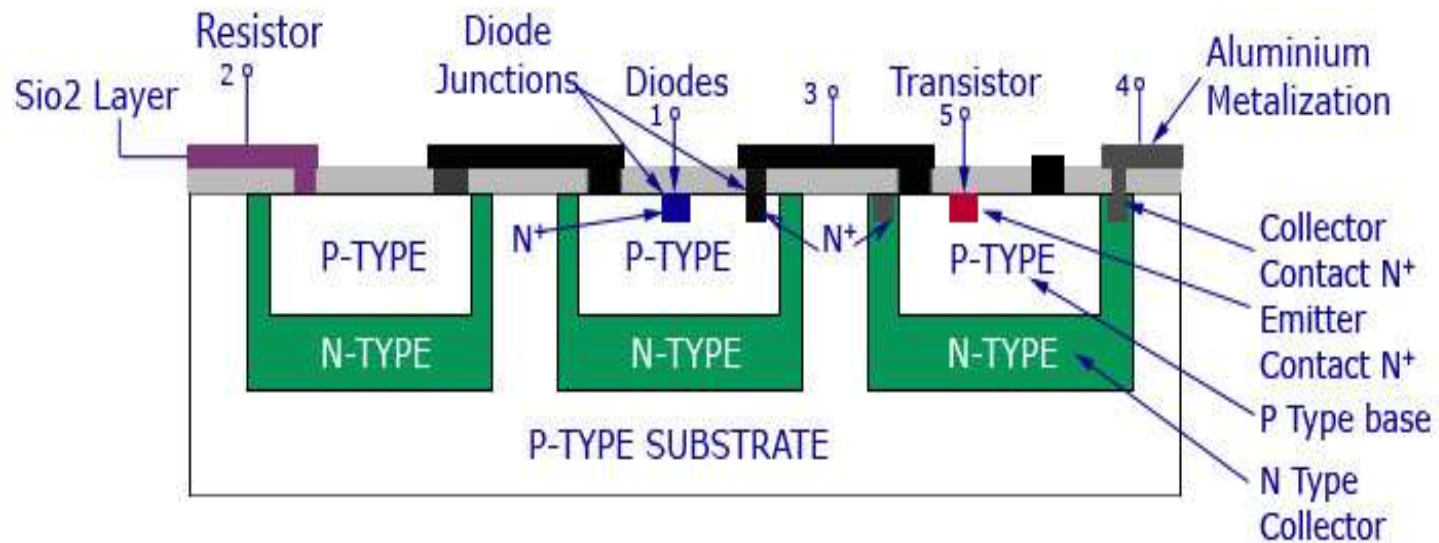
- ❑ The term monolithic is derived from Greek words monos (meaning single) and lithos (meaning stone).
- ❑ Thus a monolithic circuit is built into a single or single stone or single crystal of silicon.
- ❑ The word integrated refers to the fact that all the circuit components-transistor, diodes, registers, capacitor and their interconnections is that practical values of inductance cannot be realized .

Manufacturing Process of Monolithic ICs

- Manufacturing processes of monolithic IC using silicon planar technology can be classified as follows:
 - 1. Silicon wafer preparation
 - 2. Epitaxial growth
 - 3. Oxidation
 - 4. Photolithography
 - 5. Diffusion
 - 6. Ion implantation
 - 7. Isolation techniques
 - 8. Metallization
 - 9. Assembling and packaging process

For the manufacture and production of the monolithic IC, all circuit components and their interconnections are to be formed in a single thin wafer layer. The different processes carried out for achieving this are explained below.

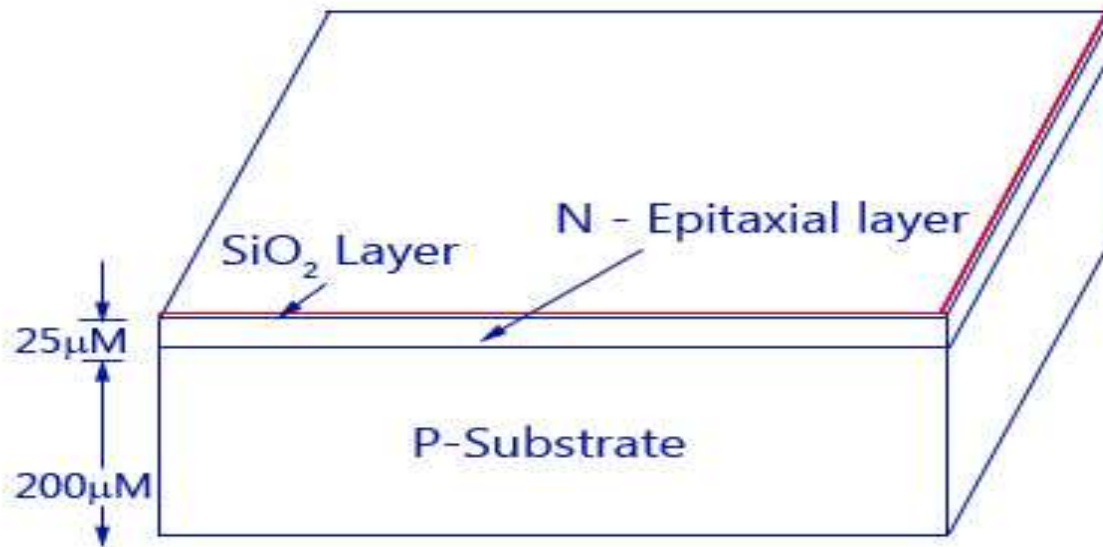
Basic Monolithic IC Cross-Sectional View



The Silicon Dioxide Insulation Layer

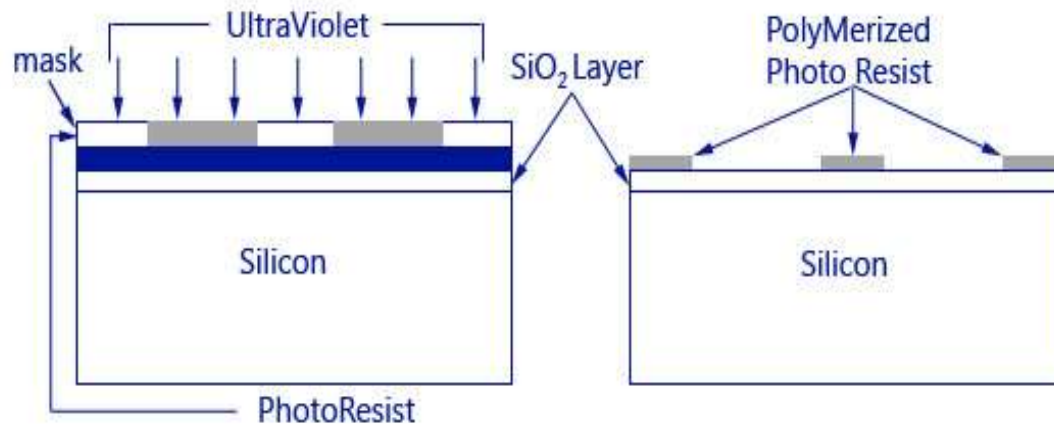
As explained above, this layer is required contamination of the N-layer epitaxy. This layer is only 1 micrometer thin and is grown by exposing the epitaxial layer to oxygen atmosphere at 1000C. A detailed image showing the P-type, N-type epitaxial layer and SiO₂ layer is given below.

Monolithic IC - Substrates and Layers

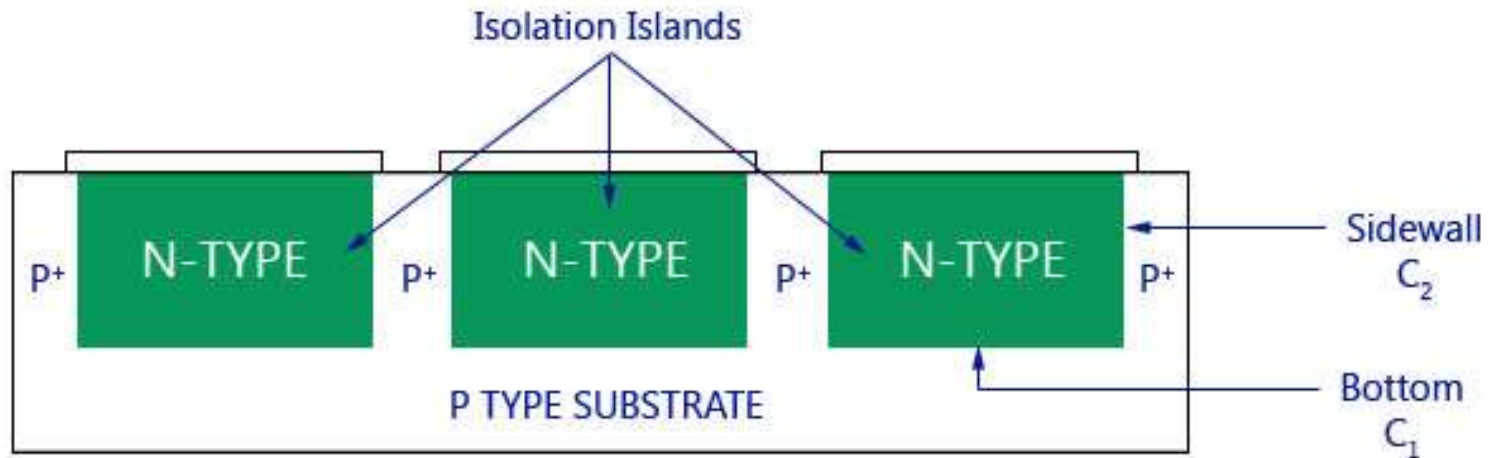


To diffuse the impurities with the N-type epitaxial region, the silicon dioxide layer has to be etched in selected areas. Thus openings must be brought at these areas through [photolithographic process](#).

Monolithic IC - Photolithographic Process



MONOLITHIC IC - ISOLATION DIFFUSION



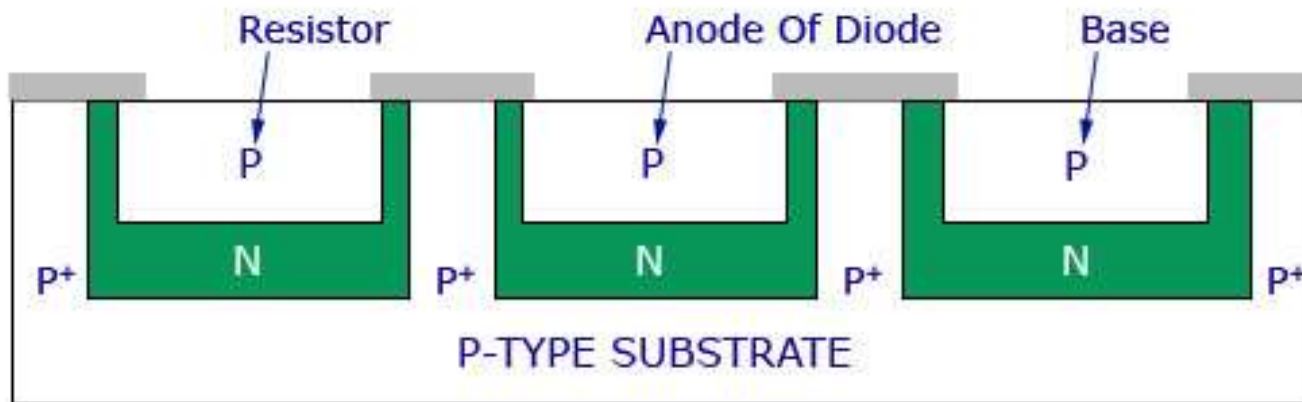
www.CircuitsToday.com

Monolithic IC - Isolation Diffusion

An effect of capacitance is produced in the region where the two adjoining isolation islands are connected to the P-type substrate. This is basically a parasitic capacitance that will affect the performance of the IC.

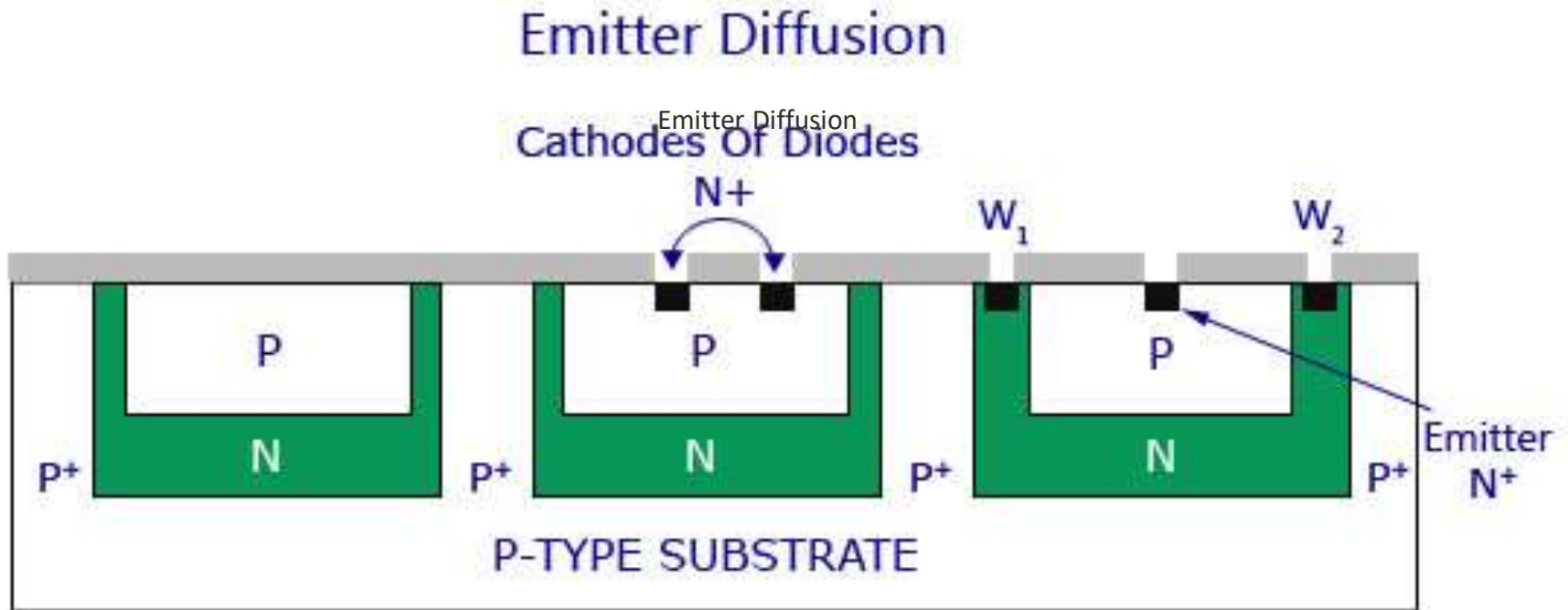
This process is done to create a new layer of SiO₂ over the wafer. P-regions are formed under regulated environments by diffusing P-type impurities like boron. This forms the base region of an N-P-N transistor or as well as resistors, the anode of diode, and junction capacitor. In this case, the diffusion time is so controlled that the P-type impurities do not reach the substrate. The resistivity of the base layer is usually much higher than that of the isolation regions.

Monolithic IC - Base Diffusion



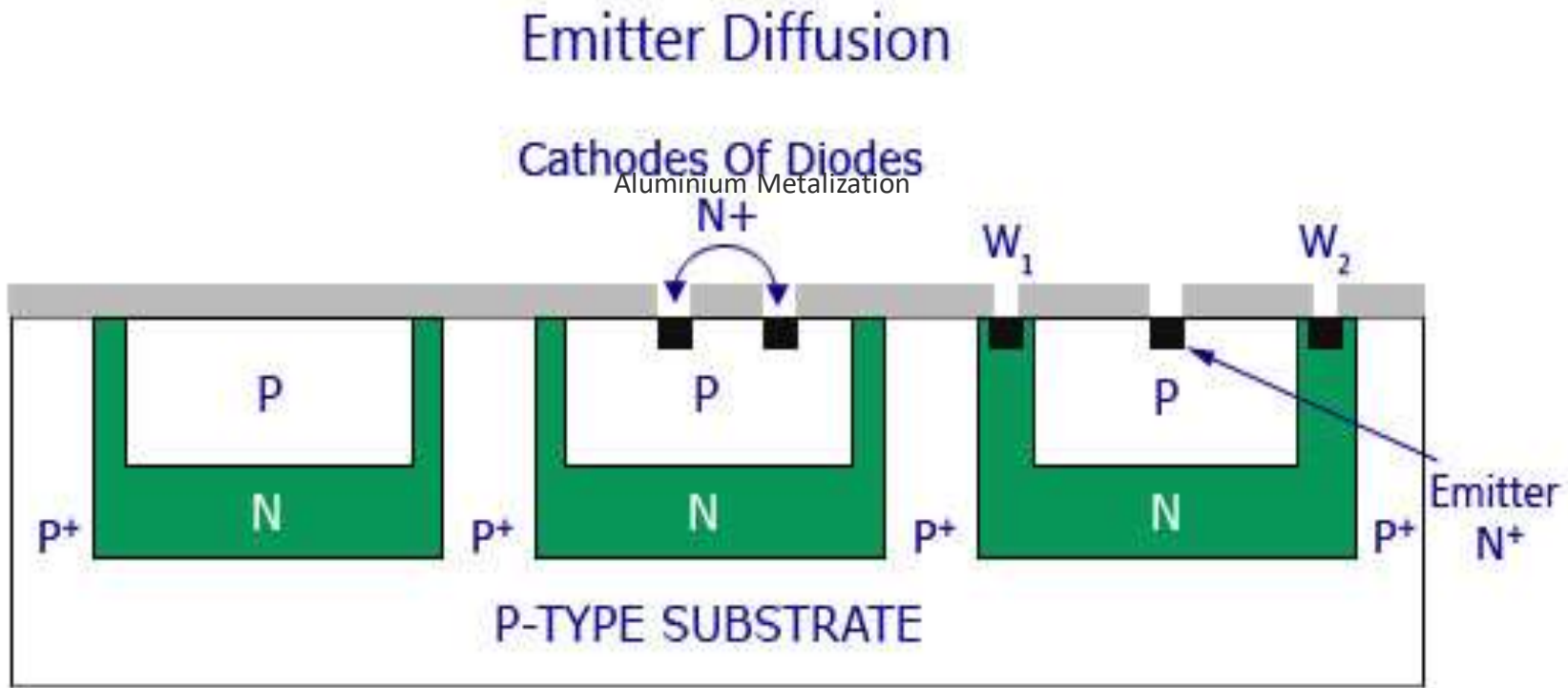
Emitter Diffusion

The transistor emitters, the cathode regions for diodes, and junction capacitors are grown by diffusion using N-type impurities like phosphorus through the windows created through the process under controlled environmental process. As shown in the figure below there are two additional windows: W1 and W2. These windows are made in the N-region to carry an aluminium metallization process.



Aluminium Metallization

The windows made in the N-region after creating a silicon dioxide layer are then deposited with aluminium on the top surface. The same photoresist technique that was used in photolithographic process is also used here to etch away the unwanted aluminium areas. The structure then provides the connected strips to which the leads are attached. The process can be better understood by going through the figure below.



These are the most significantly used IC packages is **Dual Inline Packages (DIP)**. Just like in *28-pin ATmega328*, the pins are placed in parallel to each other extending perpendicularly and laid out on a black plastic housing which is rectangular in shape. The pins are spaced at 0.1 inches. Furthermore, the package varies in size due to the difference in the number of pins in different packages. The number ranges from 4 to 64. These pins are placed in a manner that they can be adjusted on to the center of a breadboard without short-circuiting each other or even get smoldered into PCBs.

Small outline L-led package- This type has gull-wing type leads that draw out on either direction from the body in an L fashion and can be mounted directly on the board. **Quad Flat L-led Packages (QFP)-** These are similar to **SOP**. However, the only difference is that the leads are drawn out in 4 directions instead of 2 and are mounted directly on the board. They also come with a heat sink and built-in heat spreader.

Ball Grid Array (BGA) - These have solder ball arrays on the back surface of PCBs. **Fine Pitch Land Grid Array-** These have solder land arrays on the back surface of PCBs. **Wafer Level Chip Size Package-** Many Individual chips are made out of a packaged wafer that is cut out.

IC Package - Through Hole



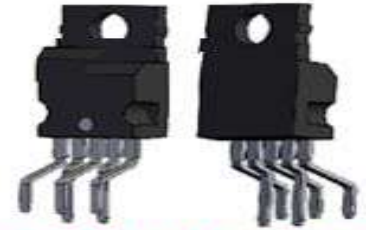
PDIP



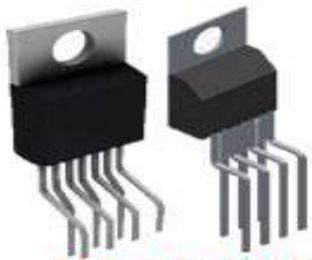
DIP



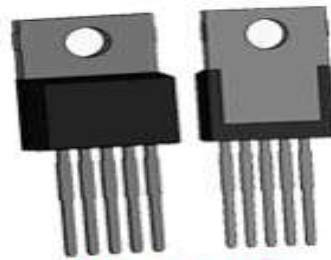
ZIP



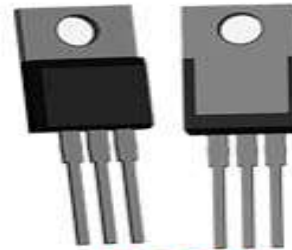
PENTAWATT



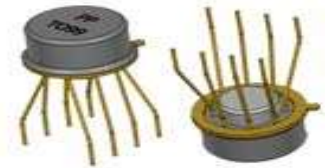
T7-TO220



TO2205



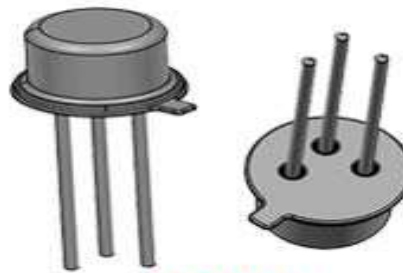
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TO99



TO92



TO18



TO03

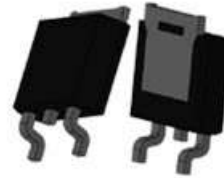
IC Package - Surface Mount



SOT23



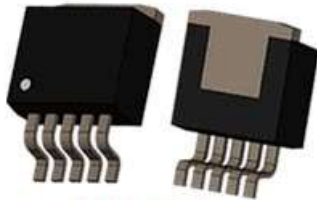
SOT223



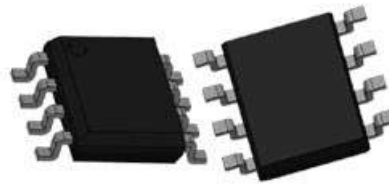
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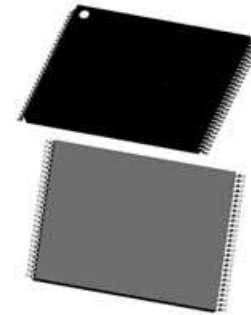
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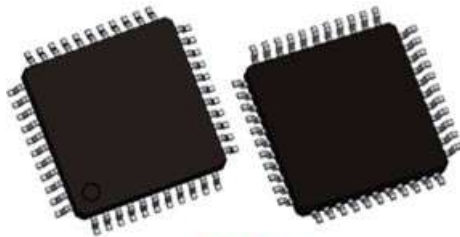
DPAK



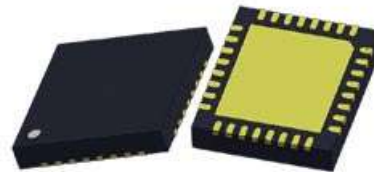
SOP



TSOP



TQFP



QFN



BGA